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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/516,583	03/24/2005	Charles Eugene Stroud	46872/308797	9939

44231 7590 06/08/2007

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EXAMINER	
PRETLOW, DEMETRIUS R	

ART UNIT	PAPER NUMBER
2863	

MAIL DATE	DELIVERY MODE
06/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/516,583	STROUD ET AL.	
	Examiner	Art Unit	
	Demetrius R. Pretlow	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/13/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-35 are rejected under 35 U.S.C. 102(a) as being by anticipated Abramovici et al. "BIST-Based Sdelay-Fault Testing in FPGAs". Abramovici et al. teach (a) applying a test pattern approximately simultaneously to a first path under test in the field-programmable gate array and a second path under test in the field-programmable gate array, wherein the first path under test and the second path under test have substantially the same propagation delays in a fault free circuit; Note page 550, left column , lines 32-34 and Note section 3.1, lines 1-9; Abramovici et al. teach receiving a first output signal indicating that the test pattern has propagated through at least one of the first path under test and the second path under test; Note section 3.1, lines 11-19; Abramovici et al. teach receiving a second output signal that indicates the test pattern has propagated through each of the first path under test and the second path under test; Note section 3.1, lines 11-19; Abramovici et al. teach determining the interval between receiving the first output signal and the second output signal; Note section 3, lines 19-27 and Abramovici et al. teach identifying a fault in at least one of the first path under test and the second path under test when the interval exceeds a threshold; Note

section 3.1, lines 22-24 and (f) causing an indication of the fault to be output. Note section 3.1, lines 22-24.

In reference to claim 13, Abramovici et al. teach a first path under test in the field-programmable gate array, the first path under test in communication with the input; a second path under test in the field-programmable gate array, the second path in communication with the input, wherein the second path has an expected propagation delay substantially the same as the first path under test; Note section 3.1, lines 8-9; and an output response analyzer (ORA) Note section 4, lines 1-12 ,in communication with the first path and the second path and operable to: determine an interval between the time a data signal propagates through the first path under test and the second path under test; Note section 3.1, lines 19-27 and identify a fault in at least one of the first path under test and the second path under test when the interval exceeds a threshold. Note section 3.1, lines 22-24.

In reference to claim 2, Abramovici et al. teach activating an oscillating signal after receiving the first output signal; deactivating the oscillating signal after receiving the second output signal; and counting the number of oscillation cycles occurring while the oscillating signal is active. Note section 3.1 , lines 15-20.

In reference to claim 3, Abramovici et al. does not explicitly teach wherein the test pattern comprises contain a high to low transition however this would be inherent to the test pattern of Abramovici et al. Note page 550, lines 32-33.

In reference to claim 4, Abramovici et al. does not explicitly teach wherein the test pattern comprises contain a low to high transition however this would be inherent to the test pattern of Abramovici et al. Note page 550, lines 32-33.

In reference to claim 5, Abramovici et al. teach generating the test pattern. Note page 550, lines 32-33.

In reference to claim 6, Abramovici et al. teach configuring the first path under test and the second path under test. Note section 3.1, lines 1-2.

In reference to claim 7, Abramovici et al. teach developing a configuration for the first path under test and the second path under test. Note section 3.1, lines 1-2.

In reference to claim 8, Abramovici et al. teach the first path under test comprises a fast path; and the second path comprises a slow path. Note section 3.1lines 15-23.

In reference to claim 9, Abramovici et al. teach 9. (original) The method of claim 1, wherein at least one of the first path under test and the second path under test comprises at least one programmable logic block (PLB) configured as an adder for computing the k-bit sum (S) of two k-bit inputs, A and B, and having a carry-in (Cin) and carry-out (Cout). Note section 3.4, lines 1-15.

In reference to claim 10 Abramovici et al. teach applying the test pattern comprises applying a raising transition at Cin and B and a 0 vector at A; and receiving the first and second output signals comprises receiving raising transition at Cout. Note Figure 6.

In reference to claim 11, Abramovici et al. teach applying the test pattern comprises applying a falling transition at Cin and B and a 1 vector at A; and receiving

the first and second signals comprises receiving a falling transition at Cout. Note Figure 6.

In reference to claim 12, Abramovici et al. teach applying the test pattern comprises applying a raising transition at Cin, a 0 vector at A, and a 1 vector at B; and receiving the first and second signals comprises receiving a falling transition at S.

In reference to claim 14, Abramovici et al. teach an oscillator; and a counter in communication with the oscillator. Note page 554, right column lines 3-5.

In reference claim 15, Abramovici et al. teach an NAND gate in communication with the first path under test; a first OR gate in communication with the second path under test; and a second OR gate in communication with the NAND gate and the first OR gate. Note Figure 3.

In reference to claim 16, Abramovici et al. teach an OR gate in communication with the first path under test; a first NAND gate in communication with the second path under test; and a second NAND gate in communication with the OR gate and the first NAN/) gate. Note Figure 3.

In reference to claim 17, Abramovici et al. teach wherein the programmable logic blocks in the first path under test and the second path under test comprise identity functions. Note page 552, left column lines 6-7.

In reference to claim 18, Abramovici et al. teach wherein each of the first path under test and the second path under test comprises at least one lookup table (LUT) and where each LUT is configured to produce a transition when the input of the LUT changes to a specified target address. Note section 3.3, lines 1-9.

In reference to claim 19, Abramovici et al. teach wherein the LUT contents of the target address comprises a 1 and the LUT contents of all other addresses comprise a 0. Note section 3.3, lines 10-13.

In reference to claim 20, Abramovici et al. teach wherein the LUT contents of the target address comprises a 0 and the LUT contents of the all other addresses comprise a 1. Note section 3.3, lines 10-13.

In reference to claim 21, Abramovici et al. teach wherein neither of the first path under test and the second path under test comprises a flip-flop. Note section 3.3, line 21.

In reference to claim 22, Abramocici et al. teach wherein each LUT comprises k inputs and each of the first path under test and second path under test comprises consecutive groups of 2k pairs of LUT's, wherein each of the groups comprises the same configuration and each pair comprises a different target address. Note section 3.3, lines 25—28.

In reference to claim 23, Abramovici et al. teach a first programmable logic block configured as an adder for computing the k-bit sum (S) of two k-bit inputs, A and B, and having a carry-in (Cin) and carry-out (Cout). Note section 3.4, lines 1-15.

In reference to claim 24, Abramovici et al. teach wherein the output response analyzer is connected to the Cout output. Note Figure 10.

In reference to claim 25, Abramovici et al. teach a second programmable logic block configured identically to the first programmable logic block, wherein the Cin input

of the second programmable logic block is connected to the B and Cout outputs of the first programmable logic block. Note Figure 6.

In reference to claim 26, Abramovici et al. teach wherein the output response analyzer is connected to the S output. Note Figure 3.

In reference to claim 27, Abramovici et al. teach a second programmable logic block configured identically to the first programmable logic block, wherein the A input of the second programmable logic block is connected to the S output of the first programmable logic block. Note Figure 6.

In reference to claim 28, Abramovici et al. teach a third programmable logic block configured identically to the first programmable logic block, wherein the Cin input of the third programmable logic block is connected to the Cout output of the second programmable logic block; and a fourth programmable logic block configured identically to the first programmable logic block, wherein the A input of the third programmable logic block is connected to the S output of the third programmable logic block, Note Figure 10.

In reference to claim 29, Abramovici et al. teach a second programmable logic block configured identically to the first programmable logic block, wherein the Cin input of the second programmable logic block is connected to the Cout output of the first programmable logic block; a third programmable logic block configured identically to the first programmable logic block, wherein the A input of the third programmable logic block is connected to the S output of the second programmable logic block; and a fourth programmable logic block configured identically to the first programmable logic block,

wherein the Cin input of the fourth programmable logic block is connected to the Cout output of the third programmable logic block. Note Figure 10.

In reference to claim 30, Abramovici et al. teach wherein the paths under test, the test pattern generator, and the output response analyzer are all contained in the same vertical self-testing area (V-STAR). Note section 5, lines 15-17.

In reference to claim 31, Abramovici et al. teach wherein the paths under test, the test pattern generator, and the output response analyzer are all contained in the same horizontal self-testing area (H-STAR). Note section 5, lines 19-22.

In reference to claim 32, Abramovici et al. teach wherein each path under test comprises a horizontal segments contained in a H-STAR and a vertical segment contained in a V-STAR, and further comprising a configurable interconnect point configured at the intersection of the V-STAR and the H-STAR connecting the said horizontal and vertical segments. Note Figure 7.

In reference to claim 33, Abramovich et al. teach wherein the test pattern generator drives the horizontal segment and the output response analyzer observes the vertical segment of the paths under test. Note Figures 7 and 8.

In reference to claim 34, Abramovici et al. teach wherein the FPGA under test comprises a plurality of parallel vertical self-testing areas (V-STAR's), and each V-STAR comprises the delay-fault testing system of claim 13. Note Figure 7.

In reference to claim 35, Abramovici et al. teach wherein the FPGA under test comprises a plurality of parallel vertical self-testing areas (H-STAR's), and each H-STAR comprises the delay-fault testing system of claim 13. Note Figure 7.

Response to Arguments

Applicant's arguments with respect to claims 1-35 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's submission of an information disclosure statement under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p) on April 13, 2007 prompted the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 609.04(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Demetrius R. Pretlow whose telephone number is (571) 272-2278. The examiner can normally be reached on Mon.-Fri. 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on (571) 272-2269. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Demetrius R. Pretlow Demetrius Pretlow 6/4/07

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